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Sometimes Hoodoo Rituals are Needed to Implement New Technology Features in OpenVPX Chassis

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Complexity of the System Solutions

- **Rapidly changing technologies have increased the system design challenge**
  - VICTORY: Vehicle Data Bus; MORA: Modular Open Radio Architecture
- **SWaPc is a Systems Concept - not just an Acronym**
  - Size, Weight, Power and Cost
- **Packaging Expertise has evolved to require System Expertise**
- **Solutions require the integration of payload boards from the Customer and Elma partners, mated with the system chassis, custom backplane and cable set using mixed I/O.**
  - Design trades offs occur at several levels, and become a Set of considerations. Commercial boards can be unknown(in design)
- **Transfer rates over the distances are new to the design**

What Gate's System Designs

- **System Design Starts with a Physical Concept Drawing**
  - Backplane transmission rate: modeling and simulation
    - End-to-end use case from: board to backplane to board
    - Materials, design techniques, fabrication method, connectors
    - Model and simulate to review performance against targets
  - Thermal simulation and modeling
    - Power In ☐ Power Out
    - Removing heat and cooling scheme
  - I/O Design and Method
    - Connector choice to match signal speed
    - Finding the connectors, and promote sources
    - Copper vs Fiber; Digital vs Analog
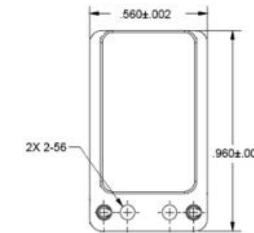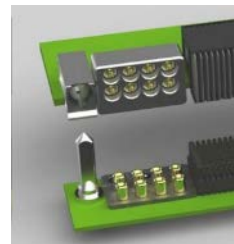   - Compatible cable solutions and contacts that are new

Design Iteration

Scope Creep
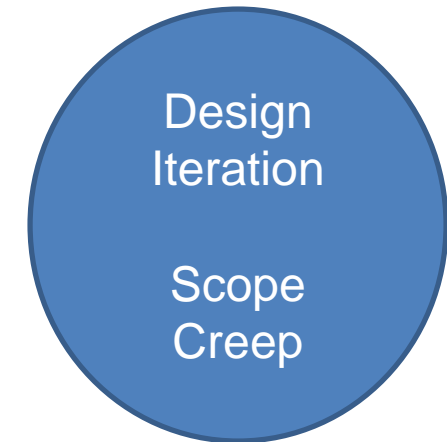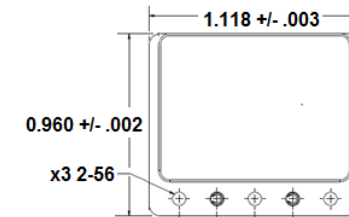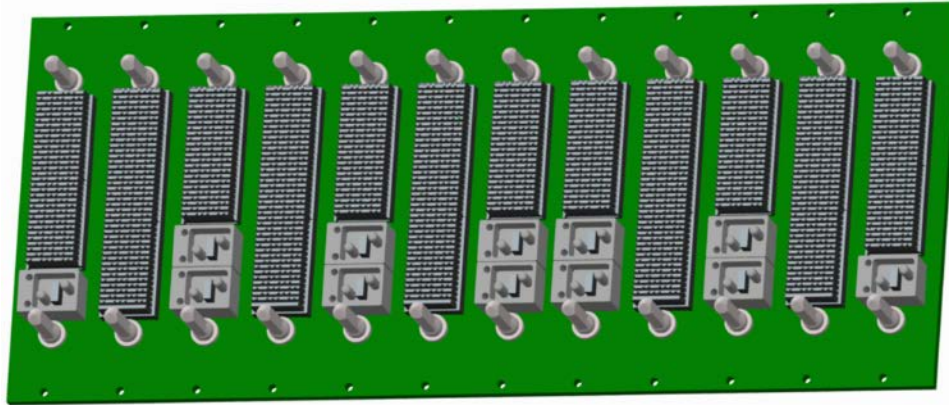
VITA 67.1 and 67.2 Module Connectors can mate with VITA 67.3 Backplane Connectors
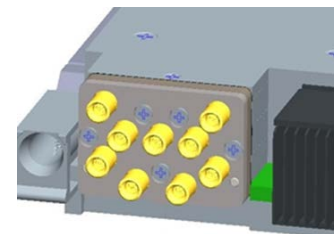
VITA 67.1

VITA 67.2

VITA 67.3C

Module 67.3c
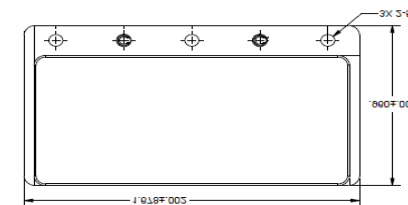
Module 67.3d

Module 67.3e

Fiber Optics – A Guiding Light

- **Reflex Photonics Transceiver with MT Ferrule**
  - Multiple Fibers per Ferrule
    - 12 to 64 per Ferrule
- **MT to Circular allows termination to the bulkhead**
- **VITA 66.4 and VITA 67.3 define Connectors**
- **Surface Mount BGA Package**
  - 40C to +85C
- **Allows Fiber I/O from VPX board to bulkhead or Board to Board**
- **Applicable for 10Gb, 40Gb, Required for 100Gb Ethernet**

Goals related to Complexity
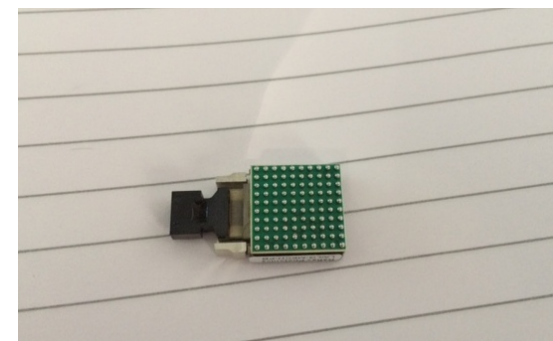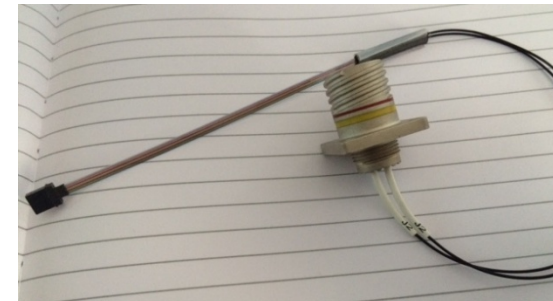
- **Mitigate development risk**

- **Find a set of resources to build a team**

- **Meet objective and threshold goals of the system design**

- **Build a supply team to vet ideas, and vet the requirements against possible solutions**

- **Progressively reduce risk thru the design effort**

Risk Elements of a Solution

- **New technology required**

- **Need to innovate**

- **Applying new standards for the first time**

- **Standards don't exist yet (not ratified)**

- **Ecosystem has not solved the application problem yet**

- **Needs components that are next generation**

- **End-to-End Solution is required – Board to Backplane to Board**

Overview - Complex Systems: H/W Convergence

- **Technology Drivers**
  - Establish the Setting and the Frame the need
- **Gating Factors and Tools**
  - Speed, Size, and Power, Performance
  - Modeling and Simulation Tools Needed
  - Dialing in the Specifications and Design
- **Component Supplier vs. Partner**
  - Finding a suitable set of partners for App
- **Integration Needs**
  - New Technology and Increased performance drives Higher Cooperation and Interchange between supply team members
  - Agile Design and Scrum techniques are necessary internally and externally

Expertise in VPX

Change Agent for Specification

Ability to Model and Simulate

Identifying Partners

Build House

Technology Trends – Where are You?

Core Technology Transition by Category

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Technology Trend Summary
Influencing Boards Backplanes and Systems

2013 Processors 2016		2013 FPGAs 2016		2013 Network 2016		2013 Storage 2016	
Generation 4 Haswell Core i7 Intel	**Generation 5 & 6** Broadwell DE – XEON (5th) SkyLake-H (6th)	**FPGA** Virtex 6 & 7 Kintex Zync	**Generation 7 & 8** Virtex, Kintex 7 UltraScale 8 Virtex, Kintex, Zync	**Ethernet** 1Gb, 10Gb 1000BASE-BX 10GBASE-KX4	**Ethernet** 1Gb, 10GbKX4 -> 10GbKR 40GB-KR	**Storage** SATA 3 SSD, Rotating 2 ½", M-SATA	**Storage** SATA 3 to PCIe SSD, Rotating 2 ½", M-SATA, M.2
GEN 4 to Gen 6 *FEATURES*		*Gen 6 to Gen 8* *FPGA FEATURES*		*Ethernet FEATURES* *1 to 10Gb to 100Gb*		*Storage FEATURES* *SATA 3 to PCIe*	
High Speed Board Design 8.125 PCIe, 6 Gb SATA, DDR3 to 10.3125 Gb Ethernet and DDR4 Memory		High Speed Backplanes 3.125 and 5.0Gb Lanes move to 10.3125 Gb Lane copper and 25Gb lane in Fiber		Backplanes: Copper and FIBER **3.125Gb to 10.3125Gb, to 25Gb**		Boards 6.0Gbs to 8Gbs PCIe	
Intel **Dual and Quad** Core I3, I5, I7 **DDR3 ECC** GPU 20 Cores Dual Gb Ethernet **SATA 3** **PCIe Gen 3** Mobile Desktop	**Generation 5** **Broadwell XEON** **8 to 16 Cores** **DDR4** **10GB-KR** Ethernet **Server Class** **Generation 6** **SkyLake** 2 or 4 Core DDR3L no ECC GPU 20 Core Faster Video RAM PCIe Gen 3 **20% faster CPU** **50% faster graphics**	**New Tool Chain** **ISE to Vivado** MGT Transceivers **12Gb/sec** **10 Gb Ethernet** Hard **PCIe** Core **Gen2** Hard MACs **Zync (SoC)** System on Chip ARM Kintex DDR3 UART USB SATA	**Vivado** **Tool Chain** MGT Transceivers 12Gb to 28Gb **100 Gb** Ethernet Hard **PCIe** Core **Gen 3** Better Clock **Zync (SoC)** **Dual ARM 64bit** **GPGPU** DDR4 A/D & D/A UART USB SATA	**1Gb Ethernet** **Prevalent** *1000BT or* *1000BASE-BX* **10Gb Ethernet** Implemented as (4) - 3.125Gb Lanes (KX4)	**1Gb Ethernet** **Prevalent** **1000BT or** **1000BASE-BX** **10Gb/40Gb** **Ethernet** **Implemented as** (1) - 10.3125Gb Or (4) 10.3125Gb Lane **100Gb Ethernet** **Defined** 25Gb/s Lane x (4)	**SATA 3Gb & 6Gb** **Rotating** 3½" and 2 ½" Disk 4TB and 2TB **Solid State** MLC, SLC 2 ½" **2TB, 512GB** New Form Factors **M-SATA** CFAST	**SATA 6Gb** **PCIe Gen 3** **Rotating** 3½" and 2 ½" Disk **6TB and 4TB** **Solid State** MLC,SLC 2 ½" **4TB, 2TB** New Form Factors M-SATA **M.2**

Networking Trends

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Faster Ethernet

100Gb

2018

40Gb-KR

10Gb-KX4

2013

2013 Network 2016
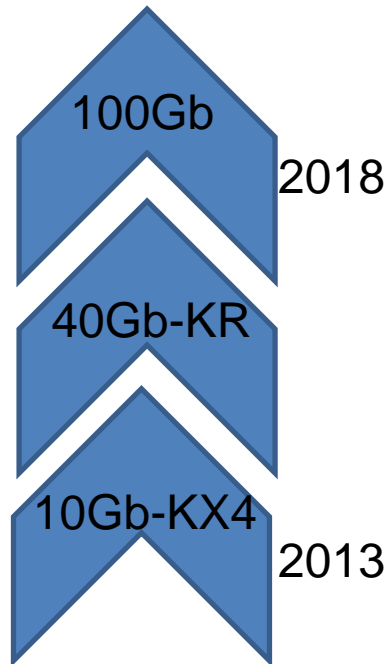
Ethernet 1Gb, 10Gb 1000BASE-BX 10GBASE-KX4	Ethernet 1Gb, 10GbKX4 -> 10GbKR 40GB-KR
Ethernet FEATURES 1 to 10Gb to 100Gb	
Backplanes: Copper and FIBER 3.125Gb to 10.3125Gb, to 25Gb	

2015

1Gb Ethernet Prevalent *1000BT or 1000BASE-BX* **10Gb Ethernet** Implemented as (4) - 3.125Gb Lanes (KX4)	1Gb Ethernet Prevalent 1000BT or 1000BASE-BX 10Gb/40Gb Ethernet Implemented as (1) - 10.3125Gb Or (4) 10.3125Gb Lane 100Gb Ethernet Defined 25Gb/s Lane x (4)

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Technology Drivers Affecting the System Solution

- **New SBC and Switch Chip Devices ---**
  - Allow new designs with more function

- **Examples Include:**
  - Servers on a Chip: Xeon – D multi-core processor
  - High speed Ethernet switches now available in 3U VPX provide necessary connectivity
  - FPGA System on Chip solution allow entire sub-systems to be placed on a 3U card

Complex Solution Summary

- **VPX is evolving to support new architectures**

- **New I/O types are being supported in VPX allowing high density fiber to be used**

- **RF I/O is supported for Mezzanines with VITA 67.3**

- **New VPX connectors will provide a path to support PCIe Gen 4**

- **High Speed backplanes can be built to support the bandwidth, and I/O connectors required by new architectures**

- **VPX systems will provide the feature set to be the platform for long life cycle systems**

VPX Road Map

- **Greater Use of Fiber Optic I/O Going Forward**
  - 100Gb Ethernet requires 25Gb per lane requiring fiber optic I/O to implement off board connections
  - Next Generation Multi-Gig connector will not support this rate
- **PCIe Gen 4**
  - Doubles bandwidth from 8 GT/s per lane to 16 GT/sec per lane ☐ BW per lane 2GB/s
- **New Multi-Gig Connector required for next generation protocols**
  - T/E connectivity indicates the design is being worked

Thank you for your time!

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